REMARKS

By this amendment, Applicant has amended claims 9 and 24. Claims 9-14 and 24-26 remain for consideration in the application. Clear support exists in the specification for the amendments. No new matter has been added.

Claim Rejections Under 35 U.S.C. § 103

Claims 9-14 and 24-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McConnell et al. (U.S. Patent No. 5,986,952) in view of Barth, Jr.et al. (U.S. Patent No. 5,134,616). Applicant traverses.

The latest Office Action asserts that a single processor is used "for carrying out the functions of the redundancy detection device 4 and of the repair device 5." (see McConnell et al., col. Applicant has repeatedly argued and shown that the use of the processor to perform such functions is eliminated by the on-chip error correction of the present claims. Specifically, the use of the processor for performing such functions is explicitly shown to be a disadvantage in the specification of the present application. Claims must be interpreted in view of the specification. See specifically paragraph 0023 of the specification which states that the memory of the present invention "is designed to include on-memory error correction circuitry logic *to free a processor such as processor 110 or other dedicated ECC circuitry/hardware from decoding ECC encoded ROM data.*" (emphasis added). It is this difference in both structure and operation, namely the performing of the error correction without use of a processor, that is one of the numerous differences between the cited references and the present claims.

Further, the Office Action attempts to use a definition of "integrated circuit" as a substitute for a definition of "integrated memory" which is the term actually used in McConnell et al. Applicant respectfully submits that the definition of "integrated memory" is not the same as that of "integrated circuit." The definition of "integrated circuit" is much more broad than any plausible definition of "integrated memory." As McConnell et al. uses the term "integrated memory" it is clearly different from the processor, as col. 4, lines 59-61 point out, wherein the processor "may be disposed on the same integrated circuit as the integrated memory or on a separate integrated circuit." It is clear from a reading of McConnell et al. that "integrated

circuit" and "integrated memory" are completely different. As is clear from a reading of the specification of McConnell et al., the "integrated memory" does not include a processor.

Applicant respectfully submits that since McConnell et al. makes it clear that error correction is performed with a processor, that McConnell et al. does not teach each and every element of the claims. Barth et al. is cited for adding on-chip ECC. Using Barth et al. for on-chip ECC, despite the fact that the Office Action already argues that McConnell et al. provides on-chip ECC (an assertion Applicant disputes), still does not teach or suggest, or offer a motivation to combine, the two references. The Office Action admits that a processor is used to carry out the functions of error correction in McConnell et al. This is not done is the claims as amended. Barth et al. does not add that element, or contain a suggestion or motivation to add that element, and as such, claims 9 and 24 are allowable. Claims 100-14 and 25-26 depend from and further define one of patentably distinct claims 9 or 24, and are also believed allowable.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2203.

Respectfully submitted,

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